Group Number and Name	**Dec14-12**
Client/Advisor	**Bong Wie**
Attendees/Role	**Sean Nichols/Leader, Chi Hoe How/Communication, Yishu Mei/Webmaster/ Meng Lu/Advisor**

Past Week Accomplishments

- **Sean -** AXI4 Stream interface complete and tested!
- **Sean -** Full register set defined and implemented in hardware
- **Sean -** Complete AXI4 Stream to Kmeans core fully assembled and simulated! -- Successful!!
- **Chi Hoe -** Decided not to use Prezi, moved to slides.com

Plan for Coming Week

- **Yishu** - Implement use of CTC hardware on ATMega 328 to control the steps of the stepper motor. This will reduce processing overhead with manually flipping bits.
- **Sean Nichols -** Add Clock Domain Crosser to cross from AXI4-Lite interface to AXI4 - Stream domain.
- **Sean Nichols** - Build custom peripheral into pipeline
- **Sean Nichols** - Fix size issues (if any), Fix timing issues (if any)
- **Sean Nichols** - Begin to test kmeans core in software
- **Chi Hoe** - Help with software

Pending Issues

- It has been noted that one stepper motor driver has been burnt out. We must do additional testing to conclude this. If so, we will need to order a new one

Individual Hourly Contributions

Name	**Hours this week**	**Hours Cumulative**
Sean Nichols	27	155
Chi Hoe How	13	101
Yishu Mei	12	99

Comments and Extended Discussions

- If the design will not fit on the Zynq FPGA, then this will be a MAJOR drawback. We will need to reconsider what logic to trim based on the specific problem. So far it appears that this could arise from two sources
    - 1) The amount of Block RAM resources available after the existing pipeline.
    - 2) The amount of logic required for tracking 16 objects simultaneously in hardware is great.
        - There simply may not be enough LUTs on the FPGA to fully implement our design
        - Routing Congestion…
    - 3) Timing may become an issue for LARGE combinatorial paths when constrained to 145MHz. We may have to look into a bit of pipelining control to fix this.